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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,878	MAGOSHI, HIDETAKA	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- Th MAILING DATE of this communication app ars on th cover sh t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 9-11, 23, 26-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

3. Referring to claim 1, Blomgren et al. have taught a system for processing a computer instruction from a source of such instructions comprising:

a. a complex instruction detector having an input and an output, the input accepting computer instructions from the source and the output being indicative of whether the instruction is a member of a set of instructions (Figure 2, elements 42 and 38, column 6, lines 28-32),

b. an address generator having an input and an output, the input accepting computer instructions from the source and the output comprising an address based on the instruction (column 7, lines 36-42),

c. a jump instruction generator having an input and an output, the input being in communication with the address generator output and the output comprising an instruction to jump to the address from the address generator (column 7, lines 36-42, the address is loaded into the instruction pointer),

d. an instruction selector having inputs and an output, the inputs being in communication with the jump instruction generator, the source and the complex instruction detector, the output comprising either the instruction from the source or the instruction from the jump instruction generator depending upon the output of the complex instruction detector (Figure 2, element 46, column 6, lines 53-56).

4. Referring to claim 2, Blomgren et al. have taught the system of claim 1, as described above, and further including a processor in communication with the output of the instruction selector (column 6, lines 60-62).

5. Referring to claim 4, Blomgren et al. have taught the system of claim 1, as described above, and wherein the source comprises a memory (Figure 3).

6. Referring to claim 5, Blomgren et al. have taught the system of claim 4 as described above, and wherein the memory includes machine instructions (Figure 3).

7. Referring to claim 9 Blomgren et al. have taught the system of claim 1, as described above, and wherein the set of instructions comprises those instructions capable of execution by a processor in a single cycle throughput (Column 2, lines 3-8, According to the definition of pipelining, an instruction is competed every cycle to maximize throughput.).

8. Referring to claim 10, Blomgren et al. have taught the system of claim 1, as described above, and wherein the complex instruction detector includes a reserved instruction exception handler (column 7, lines 32-42).

9. Referring to claim 11, Blomgren et al. have taught the system of claim 1, as described above, and wherein the system comprises a RISC-based computer chip (abstract).

10. Referring to claim 23, Blomgren et al. have taught a method of executing a program with a processor, the processor being capable of executing a set of instructions, comprising:

a. providing an original instruction from a sequence of instructions comprising a program stored in a memory (column 2, lines 8-12);

b. generating an address from the original instruction (column 7, lines 36-42);

c. generating a jump and link instruction to the address, the jump and link instruction comprising an instruction for the processor to execute instructions at the address (column 7, lines 36-42) and then return to the instruction following the original instruction in the program (column 5, lines 53-67);

d. determining whether the original instruction is a member of the set of instructions (Figure 2, elements 42 and 38, column 6, lines 28-32);

e. selecting the jump and link instruction or the original instruction based on the result of the step of determining (Figure 2, element 46, column 6, lines 53-56); and

f. providing the selected instruction to the processor (column 6, lines 60-63).

11. Referring to claim 26, Blomgren et al. have taught a system for processing computer instructions between a memory and a processor comprising:

a. a complex instruction detector connected to the memory so as to receive computer instructions from the memory and output a value indicative of whether the instruction is a member of a set of instructions (Figure 2, elements 42 and 38, column 6, lines 28-32, column 2, lines 8-12),

b. an address generator connected to the memory so as to receive computer instructions from the memory and to generate an address (column 7, lines 36-42),

c. a jump instruction generator connected to the address generator (column 7, lines 36-42),

d. an instruction selector connected to the jump instruction generator, the memory, the complex instruction detector and the processor (Figure 2, element 46, column 6, lines 53-56) so as to receive:

i. jump instructions from the jump instruction generator (Figure 2, element 46, column 6, lines 53-56);

ii. computer instructions from the memory (Figure 2, element 46, column 6, lines 53-56); and

e. the value from the complex instruction detector, whereby depending on the value from the complex instruction detector, either the jump instruction or the computer instruction is provided by the instruction selector to the processor (Figure 2, element 46, column 6, lines 53-56).

12. Referring to claim 27, Blomgren et al. have taught the system of claim 26, as described above, and wherein the set of instructions comprises those instructions which are capable of being executed by the processor without additional decoding (column 8, lines 48-50).

13. Claim 28 has nothing over claim 9 and is therefore rejected for the same reasons as set for in the rejection to claim 9.

14. Claim 29 has nothing over claim 19 and is therefore rejected for the same reasons as set for in the rejection to claim 19.

15. Claim 30 has nothing over claim 20 and is therefore rejected for the same reasons as set for in the rejection to claim 20.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 15-22, 31, 33, ad 34 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003, in view of Hennessy.

18. Claim 15 has nothing over claim 1 and is therefore rejected for the same reasons as set for in the rejection to claim 1 except for the following limitation: wherein determining whether the computer instruction is complex is performed in parallel with the steps of generating the address and generating the jump instruction. Blomgren et al. have not specifically taught wherein determining whether the computer instruction is complex is performed in parallel with the steps of generating the address and generating the jump instruction. However, Hennessy has taught that increasing parallelism increases the overall performance and instruction throughput of the system (Hennessy, pages 221-223). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Blomgren et al. determine whether the computer instruction is complex in parallel with the steps of generating the address and generating the jump instruction for the desirable purpose of increasing the overall performance and instruction throughput of the system (Hennessy, pages 221-223).

19. Referring to claim 16, Blomgren et al. have taught the method of claim 15, as described above, and wherein the computer instruction includes an opcode (column 6, lines 36-45) and an operand (column 6, lines 60-63).

20. Referring to claim 17, Blomgren et al. have taught the method of claim 16, as described above, and wherein the step of generating an address is based on the opcode of the instruction (column 7, lines 29-42).

21. Referring to claim 18, Blomgren e al. have taught the method of claim 15, as described above, and wherein the step of determining whether the computer instruction is complex comprises determining whether the computer instruction generated a reserved instruction exception (column 7, lines 29-54).

22. Referring to claim 19, Blomgren et al. have taught the method of claim 15 as described above, and wherein the address identifies computer instructions for emulating the complex computer instruction (column 7, lines 29-54).

23. Referring to claim 20, Blomgren et al. have taught the method of claim 15 as described above, and wherein the step of generating a jump instruction comprises appending a Jump and Link instruction to the address (column 7, lines 36-42).

24. Referring to claim 21 Blomgren et al. have taught the method of claim 15, as described above, and wherein the steps of generating a jump instruction and the step of determining whether the computer instruction is complex are performed before the step of selecting (column 6, lines 28-32 and 53-56).

25. Referring to claim 22, Blomgren et al. have taught the method of claim 15, as described above, and wherein the address is the same for all complex instructions (Column 8, lines 51-67, Figure 3, element 76).

26. Referring to claim 31, Blomgren et al. have taught a system for processing computer instructions comprising:

a. a source of complex and simple instructions, the simple instructions being capable of being executed by the processor and the complex instructions not being capable of being executed by the processor (abstract, column 6, lines 15-67),

b. a complex instruction detector connected to the source and an instruction selector, the complex instruction detector receiving computer instructions from the source and providing a value indicative of whether a received instruction is complex or simple (Figure 2, elements 42 and 38, column 6, lines 28-32, column 2, lines 8-12),

c. an address generator connected to the source and a jump instruction generator, the address generator receiving computer instructions from the source and, if a received instruction is complex, providing an address in a memory containing emulation instructions, whereby the emulation instructions are simple instructions and emulate the intended function of the complex instruction (column 7, lines 36-42),

d. the jump instruction generator being connected to the address generator and the instruction selector, the jump instruction generator receiving addresses from the address generator and providing a jump and link instructions to the addresses (column 7, lines 36-42),

e. the instruction selector being connected to the jump instruction generator and the complex instruction detector such that the instruction selector provides a jump and link instruction from the jump instruction generator if the instruction received from the source is complex, or provides the instruction if the instruction received from the source is simple (Figure 2, element 46, column 6, lines 53-56), and

f. a processor for receiving the instructions from the instruction selector (column 6, lines 60-63).Blomgren et al. have not specifically taught wherein the complex instruction detector operates in parallel with the address generator and the jump instruction generator. However, Hennessy has taught that increasing parallelism increases the overall performance and instruction throughput of the system (Hennessy, pages 221-223). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex instruction detector of Blomgren et al. operate in parallel with the address generator and the jump instruction generator for the desirable purpose of increasing the overall performance and instruction throughput of the system (Hennessy, pages 221-223).

27. Referring to claim 33, Blomgren et al. have taught the system of claim 31, as described above, and wherein the address generator provides a first address in response to a first complex instruction and a second address in response to a second instruction, the first and second addresses being different (column 7, lines 29-54).

28. Referring to claim 34, Blomgen et al. have taught the system of claim 31 as described above, and wherein the complex instruction detector uses routines associated with reserved instruction exceptions (column 7, lines 32-42).

29. Claims 6, 7, 8, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

30. Referring to claim 6, Blomgren et al. have taught the system of claim 1, as described above. Blomgren et al. have not specifically taught wherein the complex instruction detector, address generator, jump instruction generator and instruction selector are stored on a single computer chip. However, Official Notice is taken that it is well known that storing parts on a single computer chip speeds up communication between the parts. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex instruction detector, address generator, jump instruction generator and instruction selector are stored on a single computer chip, for the desirable purpose of minimizing communication time between the parts.

31. Referring to claim 7, Blomgren et al. have taught the system of claim 6, as described above, and wherein the address is an address in a memory located on the chip (Figure 3).

32. Referring to claim 8, Blomgren et al. have taught the system of claim 6, as described above. Bomgren et al. have not specifically taught wherein the address is an address in a memory located off of the chip. However, shifting location of parts has been held to not be a patentable difference. *In re Japikse*, 181 F.2d 1019, 1023, 86 USPQ 70, 73 (CCPA 1950). Having the address be located off chip increases the amount of memory from which the addresses can come from. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the address of Blomgren et al., be located off of the chip, as it has been held that shifting location of parts is not a patentable difference,

furthermore, having the addresses be located off chip increases the amount of memory from which the addresses can come from which increases the flexibility of the system.

33. Referring to claim 12, Blomgren et al. have taught the system of claim 1, as described above. Blomgren et al. have not specifically taught wherein the address generator includes a programmable logic array. However, Official Notice is taken that programmable logic arrays makes systems more flexible. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the address generator, as taught by Blomgren et al., be a programmable logic array, in order to increase the flexibility of the system.

34. Referring to claim 13, Blomgren et al. have taught the system of claim 12, as described above, and wherein the output of the programmable logic array depends on the opcode of the inputted instruction (column 7, lines 29-54).

35. Referring to claim 14, Blomgren et al. have taught the system of claim 13, as described above, and wherein the output of the programmable logic array depends on the operand of the inputted instruction (Column 7, lines 29-54, In order to perform a correct emulation of the instruction, it must depend on the operand. For example, in order to perform a correct division, the system must know what is being divided. When the system attempts to divide by zero, en exception is signaled which causes the emulation mode to be entered.).

36. Claims 3, 24, and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, in view of Ireton, US Patent 5,826,089, both cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

37. Referring to claim 24, Blomgren et al. have taught the method of claim 23, as described above. Blomgren et al. has not specifically taught further including providing the selected

instruction to an instruction cache of the processor. However, Ireton et al. have taught providing the selected instruction to an instruction cache of the processor (Ireton, column 4, line 64-column 5, line 17) for the desirable purpose of directly dispatching instructions to the execution core. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the selected instruction of Blomgren et al., to the instruction cache of Ireton, for the desirable purpose of directly dispatching instructions to the execution core (Ireton, column 4, line 64-column 5, line 17). '

38. Claim 3 has nothing over claim 24 and is therefore rejected for the same reasons as set forth in claim 24.

39. Referring to claim 25, Blomgren et al. have taught the method of claim 24, as described above, and wherein the step of providing an original instruction includes retrieving the instruction from a memory (Blomgren et al., column 2, lines 8-12).

40. Claim 32 is rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, in view of Ireton, US Patent 5,826,089, both cited by Applicant on the Information Disclosure Statement filed on January 13, 2003, and further in view of Hennessy.

41. Claim 32 has nothing over 24 and is therefore rejected for the same reasons as set forth in claim 24.

Response to Arguments

42. Applicant's arguments with respect to claims 15-22 and 31-34 have been considered but are moot in view of the new ground(s) of rejection.

43. Applicant's arguments filed with respect to claims 1-14 and 26-30 have been fully considered but they are not persuasive.

44. On page 14, Applicant argues in essence:

"In each of the independent claims, a selection is made between an "original" instruction (e.g., the instruction from the source in claim 1, the original instruction in claim 23, or the computer instruction in claim 26) and a "jump" instruction (e.g., the instruction from the jump instruction generator of claim 1, the jump and link instruction of claim 23, or the jump instruction of claim 26). The "jump" instruction is generated based at least in part on the "original" instruction.

In contrast, the multiplexer of Blomgren simply determines whether the CPU is operating in a RISC mode or a CISC mode without regard to whether the instruction is a member. The multiplexer does not select a jump instruction based on whether the newly-loaded instruction is a member but rather based on the value of a bit flag common to the entire chip.

Blomgren neither teaches nor suggests determining whether an instruction is a member of a set of instructions and selecting between an "original" instruction and a "jump" instruction based upon the determination."

However, Blomgren et al. have taught determining whether an instruction is a member of a set of instructions and selecting between an "original" instruction and a "jump" instruction based on the determination. In Blomgren et al., when the CPU is operating in a CISC mode, the instruction is a member of the CISC set of instructions and when the CPU is operating in a RISC mode, the instruction is a member of the RISC set of instructions. (Figure 2, elements 38 and 42, column 6, lines 28-32). Blomgren et al. determines whether the next instruction is a member of the RISC set of instructions or a member of the CISC set of instructions based on the mode bits. Once it has been determined which set of instructions the next instruction belongs, a next instruction is selected (column 6, lines 53-56). So Blomgren et al. have in fact taught determining whether an instruction is a member of a set of instructions (Figure 2, elements 38 and 42, column 6, lines 28-32) and selecting between an "original" instruction and a "jump" instruction based on the determination (column 6, lines 53-56). Therefore this argument is moot.

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

46. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

48. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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